REMARKS

The Examiner's Office Action of May 19, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application, and for the Examiner's time preparing and conducting the personal interview with Applicants' representative on April 19, 2005.

This response is being filed during appeal to attempt to overcome the pending rejections, or, at least, to reduce the issues on appeal, if deemed necessary.

Referring now to Section 1, page 2 of the Office Action, the reference to Misura et al. (*High-Performance Low-Temperature Poly-Si TFTs for LCD*) was submitted in the 9/9/02 IDS and re-submitted in the Fax dated April 15, 2004. Hence, Applicants respectfully request the Examiner to consider the Misura et al. reference. A courtesy copy of this reference is again provided herewith.

With respect to the Fax of 4/15/04 and missing translation for JP 61-31288 and JP 61-725549 and the DE 39 25085C1 with an abstract, Applicants have provided all of the above-mentioned documents in the Supplemental Information Disclosure Statement filed July 13, 2004. A search using PTO's private PAIR shows that the Supplemental IDS of July 13, 2004 has been received and entered. It is requested that the Examiner contact the undersigned if copies can still not be located at the Patent Office, so that courtesy copies can be provided for consideration by the Examiner.

With regard to Sections 2-4 on pages 2-3 of the Office Action, Applicants elected Species c, subspecies (ii) directed to silicon nitride in the Response filed September 5, 2003. According to the Examiner, the following claims are deemed as directed to Applicants-elected species: Claims 1-4, 6-9, 18, 20-22, 61-62, 64, 66-67, 69, 71-72, 74, 76-77, 79, 81-82, 84, 86-87, 89, 91-96, 102-111 and 131- 135.

Applicants note that, in the Office Action Summary (form PTO-326) dated April 19, 2004, claim 19 was summarized as a rejected claim and was omitted in the list of claims withdrawn from consideration. As claim 19 is directed to a non-elected species (i.e., ion-blocking film comprising silicon oxide), claim 19 is withdrawn.

Claims 20-22 have been amended, as shown above, to correct an obvious typographical error. As a result, claims 20-22 are now dependent from claim 17.

Applicants note that claim 112 is directed to a non-elected invention. Hence, claim 112 should be included in the list of non-elected claims in Section 4, page 3 of the Office

Action. Also, claim 112 should be deleted from the list of rejected claims in the Office Action Summary (form PTO-326) dated April 19, 2004.

Responsive to Section 4, page 3 of the Office Action, Applicants have withdrawn non-elected claims 11-13, 17, 19-60, 63, 65, 68, 70, 73, 75, 78, 80, 83, 85, 88, 90, 97-101, 112-130 and 136-139, as shown above.

Further, Applicants would like to point out to the Examiner that claims 14 and 16 have previously been cancelled as shown in the Second Supplemental Amendment filed November 1, 2002. Accordingly, claims 14 and 16 should be deleted from the list of non-elected claims in Section 4 in page 3 and in the list of pending claims in the Office Action Summary (form PTO-326) dated April 19, 2004.

With regard to Section 5 on page 3 of the Office Action, the Examiner is thanked for indicating that §112 rejections and §103 art rejections of claims 1-4, 6-9, 11-14, 16-139 based on Yamazaki et al. (U.S. Patent No. 4,786,358) are removed as a result of the claim amendments submitted in the Supplemental Amendments filed August 30, 2002 (PTO date-stamped 9/9/02) and the Second Supplemental Amendment filed November 1, 2002 (PTO date-stamped 11/01/02).

With respect to Section 6 on page 3 of the Office Action, claims 61-96 and 101-109 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time of the application was filed, had possession of the claimed invention, and as the claims contain subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, to make and/or use the invention. More specifically, the Examiner stated that new claims 61, 66, 71, 76, 81 and 86 added new limitations concerning "an active matrix display device having an active matrix circuit and a driving circuit" and limitations concerning forming "a plurality of thin film transistors using...channel regions...", and the Examiner alleged that no discussion as to a "driving circuit" or what it might be, hence it appears to be new matter of unknown meaning and scope. The Examiner further alleged that nothing about channel regions or how to produce a single transistor or a plurality thereof was shown in the specification. In response, Applicants respectfully assert that page 11, lines 3-11, page 10, lines 16-17 and Figs. 7A-7D and 8, for example, provide support for the above-discussed claimed features.

As another example, on page 12, lines 22-23 of the present specification, it is stated that the descriptions of Figs. 7A-7D detailed how an active matrix circuit for driving a liquid crystal device is produced.

In the Examiner Interview Summary dated April 19, 2005, the Examiner kindly suggested Applicants to provide examples of prior art references teaching the fundamentals of active matrix display technology and providing a definition for driving circuit. In response, Applicants submit herewith a copy of each of the following three short references that were previously submitted in IDS's:

> *1. Fujii et al. "A 10 MHz Intergrated Driver Circuit for Active Matrix LCDs Using Laser-Recrystallized Silicon TFTs" pp. 448-451, Jan. 1987, IEDM 87.*
>
> *2. Misura et al., "High-Performance Low-Temperature Poly-Si TFTs for LCD", pp. 436-439, Jan. 1987, IEDM 87.*
>
> *3. Sera et al., "High-Performance TFT's Fabricated by XeCl Excimer Laser Annealing of Hydrogenated Amorphous-Silicon Film", pp. 2868-2872, IEEE Transactions on Electron Devices, Vol. 36, No. 12, December 1989.*

Applicants have highlighted portions of the above-mentioned references that may be of interest to the Examiner.

In view of the prior art references listed above, and in view of the disclosure in Figs. 7A-7D and 8 and, e.g., page 11, lines 3-11, page 12, lines 22-23, Applicants respectfully assert that the specification is fully enabling to a person of ordinary skills in the art to which it pertains. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §112, first paragraph, rejection.

With respect to Section 8, page 5 of the Office Action, claims 19-22 and 134-135 stand rejected under 35 U.S.C. §112, second paragraph because the "ion blocking layer" in claims 19-22 has no proper antecedent basis and "a plurality of times" mismatches a single article with a plural noun in claims 134-135. In response, Applicants have withdrawn claim 19 and amended claims 20-22 to depend from 17 to overcome this rejection.

Further, Applicants have amended claims 134-135, as shown above, to correct a typographical error and to improve the clarity of the claim language. However, with respect to the phrase "a plurality of times", Applicants respectfully assert that the phrase is grammatically correct and does not need to be amended, as such a recitation would be readily known to one of skill in the art.

The Examiner asserted that claim 18 effectively recites the same limitation as claim 14. In response, Applicants have cancelled claim 18, as shown above.

Claims 32-34 stand objected to under 37 C.F.R. 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim, and claims 32-34 are alleged to be identical to claims 28-30. In response, Applicants have amended claims 32-34 to properly depend from claim 31, which should overcome this objection.

In Section 9, page 6 of the Office Action, claims 1-4, 6-9, 18-22, 110-111 and 132-135 stand rejected under 35 U.S.C. §103(a) as unpatentable over Mikio Hongou or Hongou et al. in translation (JP 57-94482 – hereafter Hongou '482), alone or alternatively in view of Nishimura et al. (JP 60-147,111A – hereafter Nishimura). Further, in Section 10, page 7 of the Office Action, claims 61-62, 66-67, 69, 71-72, 74, 76-77, 79, 81-82, 84, 86-87, 89, 91-96, 102-109 and 131 stand rejected under 35 U.S.C. §103(a) as unpatentable over Hongou, in view of Nishimura, and further in view of Matsudarra et al. (JP 60-226,042A – hereafter Matsudarra) and Miller. Finally, in Section 12, page 7 of the Office Action, claims 1-4, 6-9, 18-22, 110-111, 132-135 stand rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 1 and 5-15 of Yamazaki et al. (U.S. Patent 4,786,358) in view of Hongou and Nishimura; and, in Section 13, page 8 of the Office Action, claims 1-4, 6-9, 18-22, 110-111, 132-135 stand rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 1-44 of U.S. Patent No. 6,149,988 (Shinohara et al.).

With respect to the double patenting rejections, Applicants respectfully request that the rejections be held in abeyance until all the claims are otherwise in a condition for allowance.

With respect to the §103(a) rejections, Applicants have discussed the primary reference, Hongou '482, with the Examiner during the interview, as indicated in the Interview Summary. The Examiner's acknowledgement that Hongou '482 does not teach scanning the laser beam in the manner recited in the pending claims is greatly appreciated. For the record, however, Applicants respectfully traverse the obviousness rejections at least for the reasons provided below.

As noted in detail during the Examiner's interview, Applicants respectfully assert that Hongou '482 does not teach, disclose or suggest scanning an object with a condensed laser beam in a direction orthogonal to the recited first direction, wherein a length of the third cross section in the first direction is longer than the width of the third cross section in the direction

orthogonal to the first direction. Instead, Hongou '482 (English translation) teaches scanning a beam that is oriented in a manner perpendicular to the beam of the present invention.

As disclosed at least in Fig. 7, page 3, lines 3-6, page 8, lines 2-4 from the bottom of the page, and page 9, lines 3-11, for example, Hongou teaches scanning a beam in the same direction as the longitudinal direction of the beam spot. Further, as disclosed in Fig. 7 and its associated description in page 10, lines 1-5 of Hongou, the length of the beam spot is moved in a tangential direction of a glass disc.

To facilitate the explanation of the scanning direction of the beam spot of Hongou, Applicants are attached herewith Attachment A with a marked up Fig. 10 of Hongou showing the scanning direction marked as "A".

On the other hand, Applicants' pending claims recite a laser beam having a particular geometric shape that is scanned in a direction relative to the geometric shape of the laser beam as shown in Attachment B which shows the scanning direction shown "B". As such, Applicants' laser beam scanning in the claimed direction has a different configuration and is functionally different from that of Hongou. Applicants' claimed steps enable the treatment of a large surface area more efficiently than the beam spot of Hongou.

Applicants respectfully assert that Hongou is deficient in teaching, disclosing or suggesting at least the step of scanning an object with the condensed laser beam in a direction orthogonal to the first direction, wherein a length of the third cross section in said first direction is longer than a width of the third cross section in said direction orthogonal to the first direction, as recited in claim 1.

Further, Applicants respectfully assert that Hongou is deficient in teaching, disclosing or suggesting at least the step of scanning an object with the condensed laser beam in a direction orthogonal to the first direction, wherein a length of the third cross section in said first direction is longer than a width of the third cross section in said direction orthogonal to the first direction, and wherein the length of the third cross section in the first direction is longer than a length of the first cross section in the first direction, and the width of the third cross section in the second direction is smaller than the width of the first cross section in the second direction, as recited in independent claim 6.

Still further, Applicants respectfully assert that Hongou is deficient in teaching, disclosing or suggesting at least the step of irradiating the semiconductor layer with the condensed laser beam having a second cross section at a surface of the semiconductor layer wherein a length of said second cross section in said first direction is longer than that of said

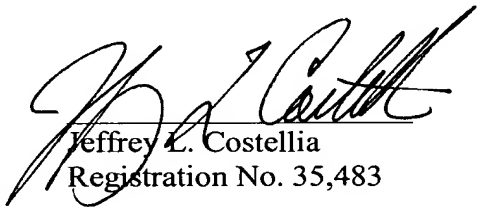
first cross section and a width of said second cross section in said second direction is smaller than that of said first cross section, as recited in independent claims 61, 66, 71, 76, 81 and 86.

As Hongou is the primary reference in all of the pending §103(a) rejections and as Hongou is deficient as noted above, the combination of Hongou with Nishimura, Matsudarra, and/or Miller is improper and a prima facie case of obviousness has not be established in the rejection of independent claims 1, 6, 61, 66, 71, 76, 81 and 86, as well as their respective dependent claims.

In order to keep prosecution history compact, and as the arguments against the rejection of the pending independent claims are deem sufficient to overcome the pending §103(a) rejections, Applicants will not address each and every rejection of the pending dependent claims. Applicants reserve the right to do so in the future, as necessary, and all arguments presented in Applicant's prior responses are also incorporated herein by reference.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
Suite 900, 401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000

A 10MHz INTEGRATED DRIVER CIRCUIT FOR ACTIVE-MATRIX LCDs USING LASER-RECRYSTALLIZED SILICON TFTs

E. Fujii, K. Senda, F. Emoto, T. Ishihara, and G. Kano

Electronics Research Laboratory Matsushita Electronics Corporation
1-1, Saiwai-cho, Takatsuki, Osaka 569, JAPAN

ABSTRACT

A monolithic integration of the horizontal driver circuit into the LCD substrate is demonstrated. The operation frequency of the TFT driver was elevated up to 10MHz by successful use of the laser-recrystallization technique. The horizontal driver circuit, of which the unit stage is composed of a D-flip flop shift register and 2-stage buffer amplifier, was fabricated on a quartz substrate together with the vertical driver and the active-matrix.

INTRODUCTION

Active-matrix LCDs have received increasing attention in view of an apprication to the small-size TVs (1). In this paper, we demonstrate for the first time the monolithic integration of the horizontal driver circuit into the LCD substrate. It is known that the operation frequency of the TFTs is strongly dependent on the grain size of the deposited polysilicon film. We show that a novel laser-recrystallization technique is effective in enlarging the grain size resulting in the dramatic increase of the operation frequency due to the increases of the electron and hole mobilities. By applying this technique, we succeeded in implementing a monolithic active-matrix LCD substrate operating up to 10MHz.

LASER - RECRYSTALLIZATION

In order to incorporate the horizontal driver circuit into LCD substrate, the operation frequency of the TFT must be elevated. To enlarge the grains of the polysilicon film is essentially requested for this purpose. The laser-recrystallization technique is known to be one of the most promising ways to enlarge the grains of the polysilicon film. However, the recrystallization technique so far developed possesses such the disadvantage that mechanical cracks are likely to occur because of the thermal expansion mismatch between the silicon and the quartz. We demonstrate here a novel technique that eliminates the above disadvantage. The principle of this technique is based on the connected-island technique (2) which is often used in zone-melting method (3). A schematic drawing which illustrates the new technique is shown in Fig.1. Note that an elliptically-shaped beam (4) is used. This method is powerful not only for eliminating cracks but also for obtaining large grains. This situation is seen in Figs.2 and 3, where the photomicrograph of the Sirtl etched surface and the TEM photograph of the recrystallized region are shown, respectively. The flat melt front rendered by an elliptically-shaped laser beam is desirable to prevent the formation of grain boundaries propagating from the island edges to the island center (5). The nallow silicon regions, through which islands are connected one another, serve as seeding region in the crystalline growth. The average grain size measured are larger than 5 μm as can be seen in Figs.2 and 3.

MONOLITHIC ACTIVE-MATRIX LCD SUBSTRATE

A schematic structure of the monolithic active-matrix LCD substrate is shown in Fig.4. The vertical driver and the horizontal driver circuits are connected to the gate and to the drain of the matrix TFTs, respectively. The circuit diagram for one stage of the vertical and horizontal drivers is shown in Fig.5. The unit stage consists of a D-flip flop shift register and a 2-stage buffer amplifier. Note that only the region for the horizontal driver is partially recrystallized by laser-annealing.

A schematic cross-sectional view of the unit inverter is shown in Fig.6. The p- and n-channel TFTs are fabricated in laser-recrystallized

448-IEDM 87

silicon islands on a quartz substarte. The fabrication steps for the horizontal driver circuit is shown in Fig.7. A deposited polysilicon film with a thickness of 0.5 μm on a quartz substrate was delineated with such the connected island structure as shown in Fig.7(a). The silicon islands were capped with a CVD silicon dioxide having a thickness of 1.0 μm. After laser-recrystallization, the silicon dioxide cap was removed and boron was implanted for threshold voltage control of n-channel TFTs. The recrystallized area outside the active device region was etched off as shown in Fig.7(b). Finally, p- and n-channel transistors were formed using the conventional CMOS process. A completed pattern of the inverter is shown in Fig.7(c). A photomicrograph of the part of the fabricated driver is given in Fig.8.

DEVICE PERFORMANCE

The typical subthreshold characteristics of the fabricated p- and n-channel TFTs are shown in Fig.9. Both of the length and the width of the channel are 10 μm. A thickness of the gate oxide is 1200Å. The threshold voltages for p- and n-channels were 1.5V and -2.5V, respectively. The electron mobility and the hole mobility calcurated from the I-V characteristics were 450cm^2/V·S and 150cm^2/V·S, respectively. It is apparent that the increase of the mobilities is due to the enlarged grains by the laser-recrystallization.

The transfer characteristics of the CMOS inverter are shown in Fig.10. It is seen that the transfer characteristics are sharp and that the threshold voltage of the inverter is well controled to be a half of VDD.

The output signal waveforms of the driver circuit are shown in Fig.11. It should be noted that the driver well operates even at 10MHz under a clock voltage of 5V.

SUMMARY

A monolithic integration of the horizontal driver circuits into the LCD substrate is demonstrated. The operation frequency of the TFT driver has been elevated up to 10MHz by successful use of the laser-recrystallization technique.

ACKNOWLEDGMENT

The authors would like to express their gratitude to Dr. I. Teramoto and Dr. M. Takeshima for valuable discussion and encouragement.

REFERENCES

(1) S. Morozumi, K. Oguchi, T. Misawa, R. Araki, and H. Ohshima, " 4.25-in and 1.51-in B/W and Full-Color LC Video Display Addressed by Poly-Si TFTs ", SID International Symposium, Digest of Technical Papers, pp.316 (1984).

(2) Y. Kobayashi, A. Fukami, and T. Suzuki, " RF Recrystallization of Polycrystalline Silicon on Fused Silica for MOSFET Devices ", J. Electrochem. Soc., Vol.131, pp.2812 (1982).

(3) M. W. Geis, H. I. Smith, J. C. C. Fan, D. J. Smith, and R. W. Mountain, " Zone-Melting Recrystallization of Si Films with a Moveable-Strip-Heater Oven ", J. Electrochem. Soc., Vol.129, pp.2812 (1982).

(4) E. Fujii, K. Senda, Y. Hiroshima, and T. Takamura, " Lateral Seeding of Silicon - on - Insulator by Using an Elliptically-Shaped Laser Beam ", Jpn. J. Appl. Phys., Vol.26, pp.1190 (1987).

(5) D. K. Biegelsen, M. M. Johnson, D. J. Bartelink, and M. D. Moyer, " Laser Induced Crystal Growth of Silicon Islands on Amorphous Substrates ", Laser and Electron-Beam Solid Interactions and Materials Processing, pp.487 (1981).

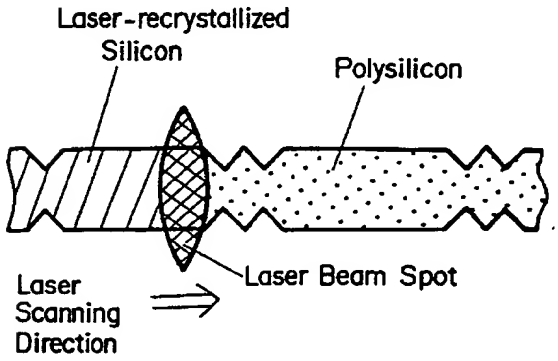


Fig.1 Schematic top view of the connected islands and laser beam spot.

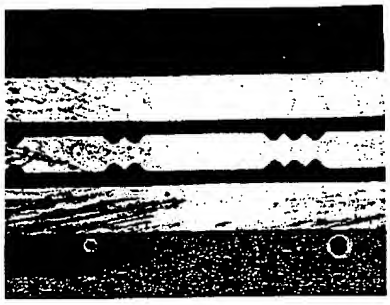


Fig.2 Photomicrograph of the Sirtl etched sample.

Fig.3 TEM photograph of the recrystallized silicon film.

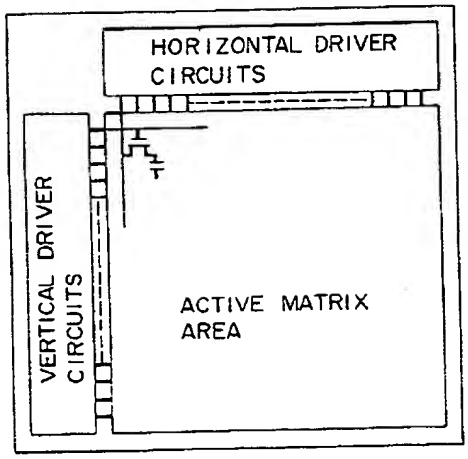


Fig.4 Schematic structure of the monolithic active-matrix LCD substrate.

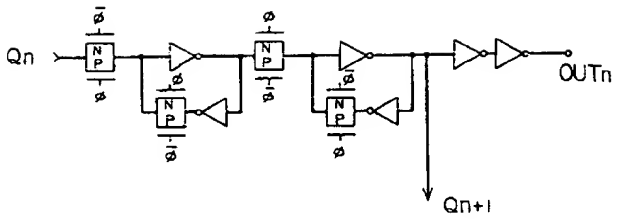


Fig.5 Circuit diagram for the fabricated driver.

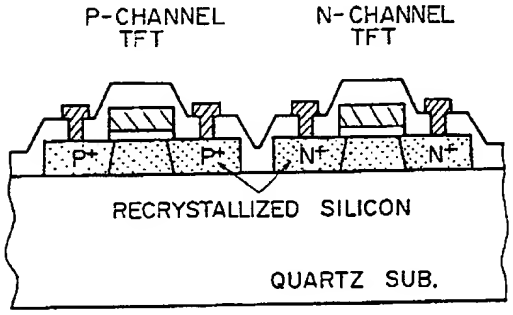


Fig.6 Schematic cross-sectional view of TFTs.

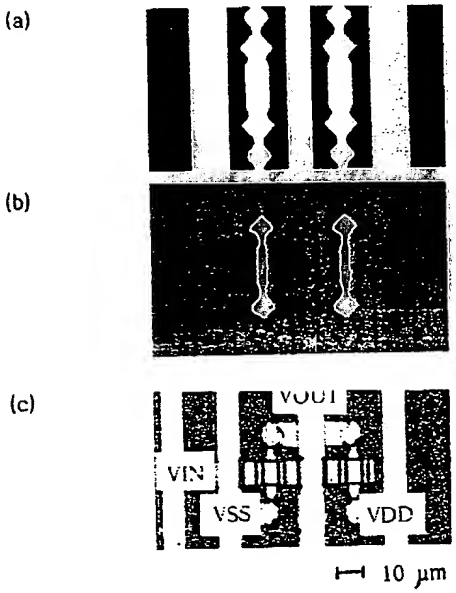


Fig.7 Process flow of the CMOS inverter.

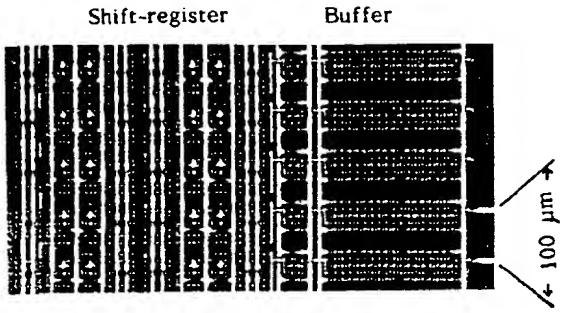


Fig.8 Photomicrograph of the fabricated driver.

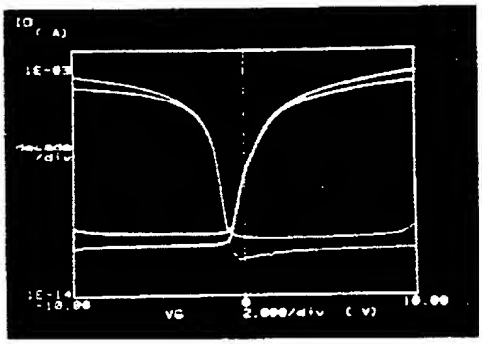


Fig.9 Subthreshold characteristics of the p-channel and n-channel TFTs of the same size of W/L=10/10 under |VD| =5,10V.

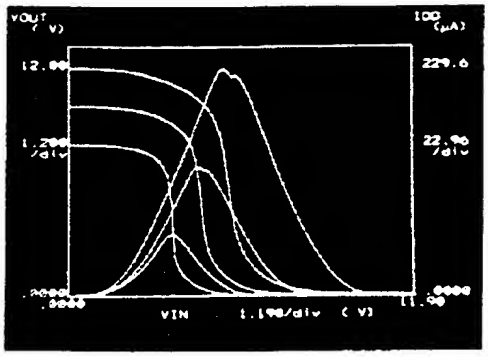


Fig.10 Transfer characteristics of the fabricated inverter under VDD=8,10,12V.

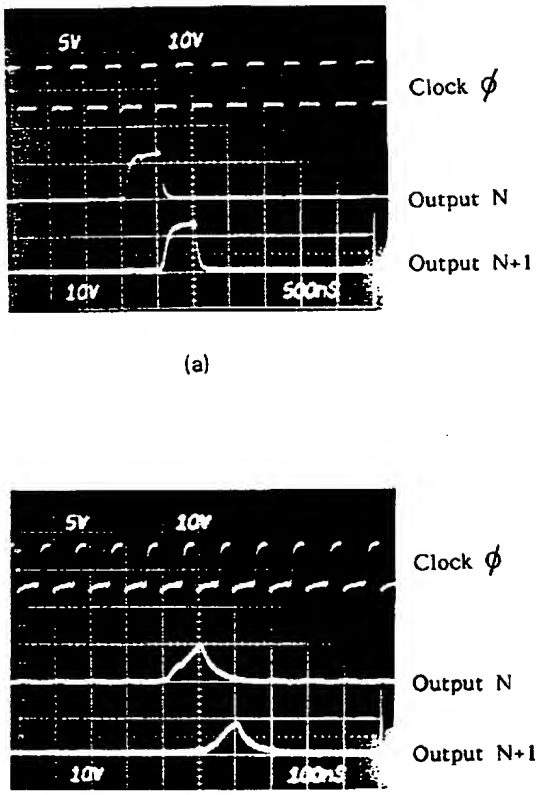


Fig.11 Clock ϕ and output signal waveform at (a) 2MHz and (b) 10MHz frequencies under VDD=14V.

High-Performance TFT's Fabricated by XeCl Excimer Laser Annealing of Hydrogenated Amorphous-Silicon Film

KENJI SERA, FUJIO OKUMURA, MEMBER, IEEE, HIROYUKI UCHIDA, SHINJI ITOH, SETSUO KANEKO, AND KAZUAKI HOTTA

Abstract—High-performance staggered a-Si:H and poly-Si thin-film transistors (TFT's) have been successfully fabricated by XeCl excimer laser annealing of a-Si:H films. The field effect mobility of poly-Si TFT is 102 $cm^2/V \cdot s$, and that of a-Si:H TFT is 0.23 $cm^2/V \cdot s$. Their drain current ON/OFF ratios are over 10^6. Except for the crystallization, the fabrication process was the same for both of them. This process appears extremely promising for the integration of matrix elements and peripheral drivers in a single substrate.

I. Introduction

RECENTLY, there has been a growing interest in active-matrix liquid-crystal displays (AMLCD's) addressed by TFT's. For such applications, a-Si:H TFT's have been attracting much attention in recent years. However, the carrier mobility for a-Si:H, which is less than 1 $cm^2/V \cdot s$, is unsuitable for peripheral circuits as videoscanners, where fairly high mobility is required. In order to avoid the difficult task of connecting an active element with external drivers, several research groups have fabricated AMLCD's with integrated drivers using poly-Si TFT's [1], [2]. One of the disadvantages of poly-Si TFT's is their high processing temperature, which requires the use of an expensive substrate. To overcome this problem, Sameshima *et al.* developed a poly-Si TFT fabricated by excimer laser annealing of a-Si:H film [3]. However, the high leakage current of the poly-Si TFT's is not yet suitable for active elements.

This paper presents a new, fully integrated AMLCD technology that employs staggered a-Si:H TFT's and excimer laser annealing, as shown in Fig. 1. To realize a fully integrated AMLCD, the combination of a-Si:H TFT's for active elements and poly-Si TFT's for peripheral circuits is the most suitable method. The staggered structure has the additional advantage of reducing leakage current. In this fabrication process, both a-Si:H TFT's and poly-Si TFT's are fabricated with the same process, except for the laser annealing step. Additional doping processes are no longer required, because doping is achieved by melting an n^+-a-Si:H layer. Since all processing temperatures are below 260°C, it is possible to use a cheap glass. This process is also free from several problems which usually occur in high-temperature processes. Superior hydrogen passivation is obtained for the poly-Si film by the use of an a-Si:H film as a starting material.

Manuscript received December 13, 1988; revised August 30, 1989.
The authors are with the Optoelectronics Research Laboratories, NEC Corporation, Miyamae-ku Kawasaki 213, Japan.
IEEE Log Number 8931490.

II. Device Fabrication

Fig. 2 shows the fabrication process for a-Si:H TFT's and poly-Si TFT's with the excimer laser annealing method. A 500-Å sputtered Cr layer and a 300-Å n^+-a-Si:H layer were deposited on a glass substrate and etched to define the source/drain electrodes. An undoped a-Si:H film of 1500 Å was deposited by the RF-glow discharge method at below 260°C. The a-Si:H layer was locally crystallized by excimer laser annealing for the poly-Si TFT's. The excimer laser annealing method is discussed later in detail. After annealing, both the crystallized and noncrystallized a-Si:H films were plasma etched at the same time to define island patterns. An additional 3000-Å RF-glow discharge SiN_x film as a gate insulator was deposited at 0.12 W/cm^2 RF-power density, which was followed by contact etching. A 2000-Å sputtered Cr layer was used for metallization.

The excimer laser annealing process was carried out in a vacuum chamber at room temperature. A sample was placed in the chamber mounted on an x–y–z pulsed stage. The laser beam was focused on the Si surface through a lens and quartz window. The laser-energy density was controlled by varying the distance between the lens and Si surface, using a z-pulsed stage. The laser energy density, used in the crystallization process, was between 140 and 160 mJ/cm^2 per pulse. The chamber was pumped out to high vacuum to avoid contamination and oxidation. The XeCl excimer laser system produces 308-nm light pulses with a pulsewidth of 35 ns. The pulse energy was 100 mJ/shot. The laser beam size was 5 × 10 mm on the surface of the sample and was clocked at 10 Hz. The development of this laser system was reported previously [4].

III. Results

A. a-Si:H TFT

Staggered a-Si:H TFT's are inferior to inverted-staggered a-Si:H TFT's in terms of electron mobility and

0018-9383/89/1200-2868$01.00 © 1989 IEEE

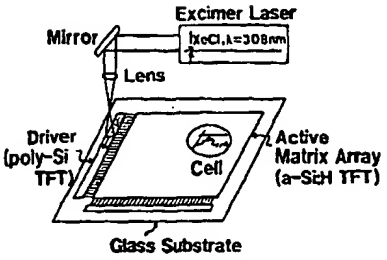


Fig. 1. Structure of AMLCD with peripheral drivers.

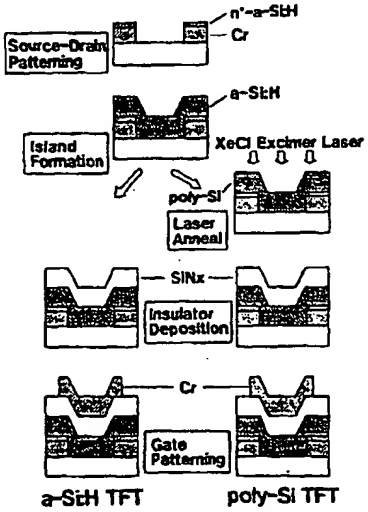


Fig. 2. Flowchart of the fabrication process for a-Si:H TFT and poly-Si TFT with excimer laser annealing method.

threshold voltage. This is mainly due to the fact that the plasma damage to the a-Si:H film during the SiN_x deposition degrades the TFT performance. However, the electrical characteristics of SiN_x degrade with decreasing RF-power density. This is the reason why the electron mobility degrades at low RF-power density. In order to determine the optimum RF-power density, the staggered a-Si:H TFT characteristics were monitored at various RF-power densities. Fig. 3 shows the field effect mobility μ_{eff} and the threshold voltage V_T as a function of RF-power density. These graphs clearly show that V_T becomes lower and μ_{eff} becomes higher with decreasing RF-power density. By optimizing RF power, significant improvement was obtained in the a-Si:H TFT's characteristics. The maximum field-effect mobility of the a-Si:H TFT was 0.23 $cm^2/V \cdot s$.

B. Poly-Si TFT's

TFT output characteristics (I_D-V_G) at various laser intensities are shown in Fig. 4. The channel width and the channel length were 40 and 20 μm, respectively. The drain voltage was 10 V. The intensities of the XeCl excimer laser were 160 mJ/cm^2, 147 mJ/cm^2, and no irradiation, respectively. Threshold voltage V_T and field effect mobility μ_{eff} were estimated from the $\sqrt{I_D}$-V_G characteris-

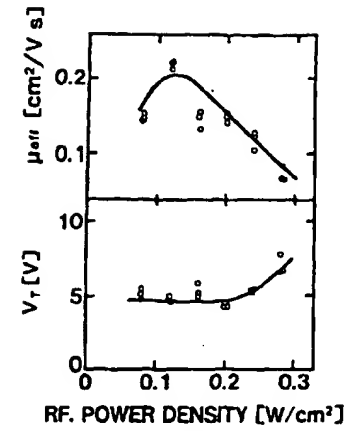


Fig. 3. Mobility and V_T as functions of RF power density in the gate insulator deposition.

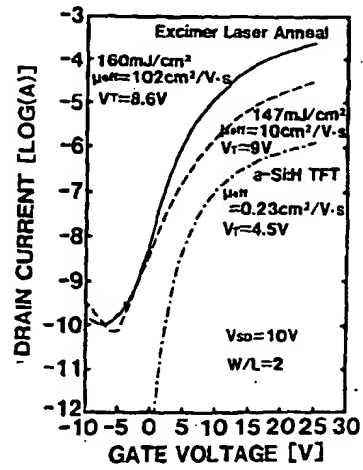


Fig. 4. The I_D-V_G characteristics of TFT's with various laser intensities V_D = 10 V, W/L = 40 μm/20 μm.

tics. The field-effect mobility μ_{eff} was calculated to be 102 $cm^2/V \cdot s$ at 160 mJ/cm^2, 10 $cm^2/V \cdot s$ at 141 mJ/cm^2, and 0.23 $cm^2/V \cdot s$ at no irradiation. The threshold voltage was calculated to be about 8 V at laser irradiation and 4.5 V at no irradiation. In this way, the TFT characteristics were improved with increasing laser intensity. In this TFT, leakage current reduction has been achieved by employing the staggered structure. The ON/OFF ratio for the drain current was over 10^6. I_D-V_D characteristics for a poly-Si TFT produced with 160 mJ/cm^2 irradiation are shown in Fig. 5.

IV. Discussion

A. Crystallization by Excimer Laser

When an a-Si:H thin film was irradiated by a pulsed excimer laser, since the absorption coefficient of the a-Si:H was 1×10^6 cm^{-1} at 308 nm, the laser energy was absorbed within 200 Å. Fig. 4 shows a cross-sectional TEM micrograph of film irradiated at 160-mJ/cm^2 intensity. In this figure, it is clearly observed that only the

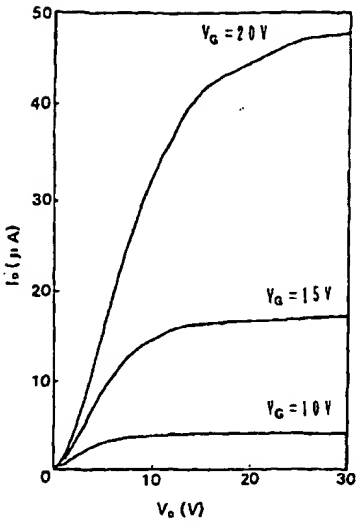


Fig. 5. The I_D-V_D characteristics of TFT's at 160 mJ/cm² irradiation.

top 150 nm of the film was crystallized by a laser pulse at 160 mJ/cm². The crystallized layer was divided into two layers, a 500-Å-thick upper large-grain poly-Si layer and a 1000-Å-thick lower microcrystalline layer. The grain size was about 200 nm at the upper layer and less than 30 nm at the lower layer. No damage was observed at the interface of the glass and the a-Si:H film. From our experiment, the upper layer thickness decreases with decreasing laser energy density without decreasing the lower microcrystallized layer thickness. Only the microcrystallized layer was observed in the irradiated film at 130 mJ/cm², which coincides with the melt-threshold energy density reported by Sameshima *et al.* [5]. Based on the results, we concluded that this double-layer crystallization is mainly due to the difference in crystallization processes. The upper layer was crystallized with a melt-growth process and the lower layer was crystallized with a solid-phase growth process. Explosive release of hydrogen atoms occurred at above 200 mJ/cm². This caused Si film quality degradation. These results indicate that a suitable intensity was between 140 and 180 mJ/cm².

B. Poly-Si TFT Characteristics

The grain size, produced by an excimer laser crystallization, was around 200 nm, as shown in Fig. 6. Small round grains were obtained by the laser annealing, in contrast to the columnar grains produced by a conventional LPCVD. In spite of a small size grain, excellent characteristics were obtained. The potential barrier height at the grain boundary (0.05 eV) in the laser crystallized poly-Si, which was determined by the temperature dependence of the ON current, is smaller than that of the LPCVD poly-Si grains (>0.1 eV). The reason for the small potential barrier height seems to be superior hydrogen passivation.

Since the excimer laser annealing is a local-heating process, optimization of both the thickness of a-Si:H and

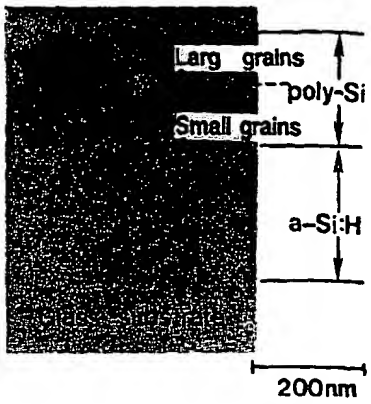


Fig. 6. Cross-sectional TEM micrograph of a-Si:H film irradiated by XeCl excimer laser (308 nm, 160 mJ/cm²).

then n⁺-a-Si:H thickness are required to obtain a good source–drain contact. Actually, slightly weak contact characteristics were observed, as shown in Fig. 5, because these optimizations were not enough.

C. Leakage Current

Conventional coplanar structure poly-Si TFT's have an anomalous leakage current problem. According to the analysis of the leakage current carried out by several research groups, the major factor which determines the leakage current is field-enhanced emission via grain boundary traps [6], [7]. Their model was developed based on the coplanar poly-Si TFT. The energy-band diagram in the drain depletion region, including the grain boundary trap level, is shown in Fig. 7(a). When the surface is accumulated, field emission current flows through grain boundary traps between the p accumulation layer and the n⁺ drain. This trap-assisted emission current is predominantly observed at the high drain voltage V_D. In contrast, the thermal emission current via grain boundary traps, which depends only weakly on V_D, is not significant [6], [7]. Therefore, as has been suggested in the literature, the reduction in the electric field strength in the drain depletion region is the most effective method to decrease the leakage current [8]. The electric field strength modification can be accomplished by using a lightly doped drain-source (LDD) structure, which is widely used to reduce the hot-electron effect in bulk MOSFET's. However, a conventional LDD structure would require additional fabrication processes.

On the other hand, the staggered structure is suitable for the reduction of electric field strength, because it forms a vertical micro LDD structure automatically. This structure has a sufficient ability to reduce leakage current without degrading the ON current. Fig. 7(b) shows an energy-band diagram for the staggered structure. The staggered structure weakens the field strength and thereby reduces the leakage current. Since the offset distance is less than a micron, it does not degrade other characteristics, such as the mobility and the threshold voltage.

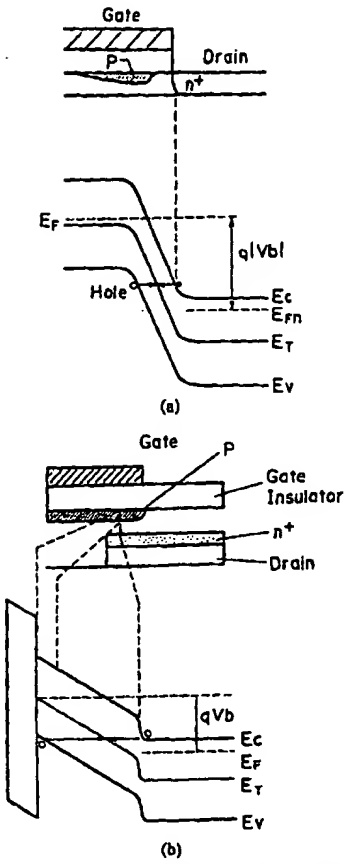


Fig. 17. The band model of TFT drain region based on carrier emission via grain boundary traps. (a) Coplanar structure, (b) staggered structure.

Fig. 8 shows a comparison between leakage current characteristics in conventional structure poly-Si TFT's and staggered structure poly-Si TFT's. Both of them were fabricated using excimer laser annealing. The gate voltage V_G was chosen so that the drain current was a minimal value. As this graph shows, the coplanar-structure TFT leakage current is increasing rapidly with increase in drain voltage. However, the staggered-structure TFT leakage current was stable up to 30 V. This current increase is due to the field emission current as mentioned above. Current-voltage dependence coincides with the theoretical expression. Leakage current has been reduced to 1×10^{-10} A (5×10^{-12} A/μm) at $V_D = 20$ V which is more than two orders of magnitude lower than that in the conventional structure. From these results it is obvious that this structure is suitable for reduction of leakage current.

V. Conclusions

A new fully integrated AMLCD technology, which consists of staggered a-Si:H TFT's for active elements and excimer laser annealed poly-Si TFT's for the peripheral circuits, has been proposed. Except for the excimer laser annealing process, both a-Si:H TFT's and poly-Si TFT's were fabricated at the same time in a single substrate. The improvements of the a-Si:H TFT characteristics were obtained by optimizing the RF-power density at gate insulator deposition. The high field-effect mobility (102 cm^2/V · s) is sufficient for the peripheral circuits. The ON/OFF current ratio ($>10^7$) of the a-Si:H TFT is high enough for the switching elements. Moreover, leakage current characteristics for poly-Si TFT's were improved by employing a staggered structure.

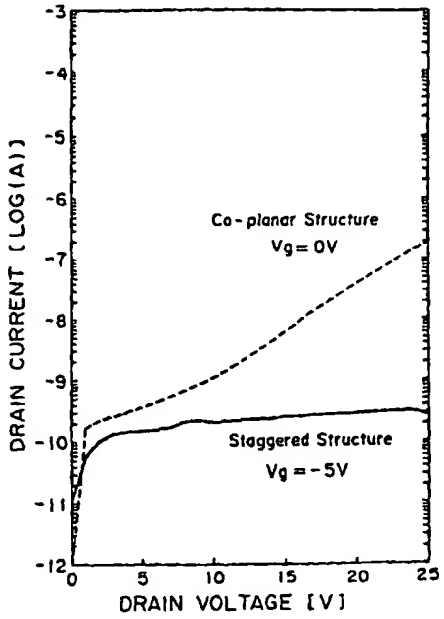


Fig. 8. The comparison of leakage current characteristics in coplanar structure and staggered structure.

Since the excimer laser annealing does not cause any damage to the glass substrate, it allows us to use a cheaper glass substrate. These result in low production cost. Moreover, peripheral driver integration avoids the interconnection problem.

Acknowledgment

The authors wish to thank Dr. M. Sakaguchi, Dr. T. Saitoh, C. Tani, and Dr. N. Nishida for their support, M. Arai, K. Sumiyoshi, and H. Asada for their valuable comments, M. Ishii for her technical support, and the other members of Display Device Research Laboratories for their helpful advice.

References

[1] S. Morozumi, K. Ogichi, T. Misawa, R. Araki, and H. Oshima, "B/W and color video displays addressed by poly-Si TFT's," in *SID'83 Dig.*, 1983, p. 156.

[2] A. Mimura *et al.*, "High performance low-temperature poly-Si TFT's for LCD," *IEDM Tech. Dig.*, p. 436, 1987.

[3] T. Sameshima, M. Sekiya, and S. Usui, "XeCl excimer laser annealing used in the fabrication of poly-Si TFT's," *Late News Abst. ICSSDM*, 17th C-3-8LN, 1985, pp. 12-13.

[4] S. Itoh, M. Arai, and K. Hotta, "200-ns long laser pulses from a simple UVpreionized XeCl excimer laser using a new charge-transfer circuit," in *CLEO'87 Tech. Dig.*, 1987, p. 326.

[5] T. Sameshima, S. Usui, and H. Tomita, "Fabrication of heavily doped polycrystalline silicon film using laser doping technique," *Japan. J. Appl. Phys.*, vol. 26, no. 10, pp. L1678–L1680, Oct. 1987.
[6] J. G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerje, "Anomalous leakage current in LPCVD polysilicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, no. 9, pp. 1878–1884, Sept. 1985.
[7] S. K. Madan and D. A. Antoniadis, "Leakage current mechanisms in hydrogenated-passivated fine-grain polycrystalline silicon on insulator MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, no. 10, pp. 1518–1528, Oct. 1986.
[8] S. Seki, O. Kogure, and B. Tsujiyama, "Laser-recrystallized polycrystalline film thin film transistors with low leakage current and high switching ratio," *IEEE Electron Device Lett.*, vol. EDL-8, no. 9, pp. 434–436, Sept. 1987.

*

Kenji Sera was born in Hiroshima, Japan, on March 5, 1961. He received the B.E. degree and the M.E. degree in electronic engineering from Osaka University in 1983 and 1985, respectively.

He joined NEC Corporation in 1985 and is now a Research Member of the Display Device Laboratory of Optoelectronics Research Laboratories. He has been engaged in the research and development of polycrystalline silicon TFT's.

Mr. Sera is a member of the Japan Society of Applied Physics.

*

Fujio Okumura (M'88) received the B.S. and M. S. degrees in electrical engineering, both from Yokohama National University, Yokohama, Japan, in 1978 and 1980, respectively.

In 1980, he joined the Central Research Laboratories, Nippon Electric Co., Ltd., Kawasaki, Japan. He has been engaged in research and development of amorphous silicon and polysilicon thin film devices. He is now a Supervisor of the Display Device Research Laboratory, Optoelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan.

Mr. Okumura is a member of the Institute of Electrical and Electronics Engineers.

*

Hiroyuki Uchida was born in 1956. He received the B.E. degree in physical electronics and the M.E. degree in applied electronics from Tokyo Institute of Technology in 1980 and 1982, respectively.

He joined NEC Corporation in 1982 and is now a Research Member of the Display Device Laboratory, Optoelectronics Research Laboratories. He has been engaged in the research and development of hydrogenated amorphous Si material and its application to large area input-output devices.

Mr. Uchida is a member of the Japan Society of Applied Physics.

Shinji Itoh was born in Yamagata, Japan. He received the B.S. degree in physics from Sophia University and the M.E. degree in physical engineering from the University of Electrocommunication.

He joined NEC Corporation in 1983 and is now a Research Member of the Optoelectronics Research Laboratories. He has been engaged in the research and development of excimer laser.

Mr. Itoh is a member of the Japan Society of Applied Physics.

*

Setsuo Kaneko was born in Kanagawa prefecture, Japan, on January 31, 1950. He received the B.S. and M.S. degrees in electronic engineering both from Tohoku University, Sendai, Japan, in 1973 and 1975, respectively.

In 1975, he joined the Central Research Laboratories, Nippon Electric Co., Ltd., Kawasaki, Japan, where he has been engaged in the research and development of semiconductor materials preparation and amorphous silicon devices. He is now a Research Manager of the Display Device Research Laboratory, Optoelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan.

Mr. Kaneko is a member of the Japan Society of Applied Physics.

*

Kazuaki Hotta was born in Fukushima, Japan, on December 10, 1945. He received the B.S. and M.S. degrees from Tohoku University, Sendai, Japan, in 1968 and 1970, respectively.

In 1970 he joined NEC Corporation and is now an Assistant Manager of the Optoelectronic Equipment Research Laboratory, Optoelectronics Research Laboratories. As a manager, he has been engaged in the research and development of gas lasers, such as discharge excited rare-gas halide excimer laser and CO_2 laser.

Mr. Hotta is a member of the Japan Society of Applied Physics, the Institute of Electrical Engineers of Japan and the Institute of Electronics, Information, and Communication Engineers of Japan.

High-Performance Low-Temperature Poly-Si TFTs for LCD

A. Mimura, N. Konishi, K. Ono, J. Ohwada, Y. Hosokawa,
Y. A. Ono, T. Suzuki, K. Miyata, and H. Kawakami

Hitachi Research Laboratory, Hitachi, Ltd.
4026 Kuji-cho, Hitachi, Ibaraki, 319-12, Japan

ABSTRACT

High-performance low-temperature poly-Si TFTs were developed by a 600 ℃ process so that a glass substrate could be utilized. To achieve low threshold voltage (V_{TH}) and high field effect mobility (μ_{FE}), effective hydrogenation using a thin poly-Si gate was employed. Furthermore, active layer poly-Si deposition conditions by LPCVD were optimized. Thinning the gate poly-Si was very effective in reducing V_{TH} by hydrogenation. Crystallinity of poly-Si after thermal annealing at 600 ℃ depended closely on the poly-Si deposition temperature and was a maximum at 550-560 ℃. The developed TFTs, with poly-Si deposited at 550 ℃ and a 1000 Å gate, had a V_{TH} of 6.2 V and μ_{FE} of 37 $cm^2/V \cdot s$. These TFTs were successfully applied to LCDs with fully integrated drive circuits.

INTRODUCTION

Thin film transistors (TFTs) on transparent substrate are very important for making the active matrix type liquid crystal displays (LCD). Poly-Si TFTs have a high field effect mobility (μ_{FE}), a potential to realize very large area LCDs [1], and a capability for peripheral drive cricuits integration [2-4]. Peripheral circuits integration leeds to reduction of external drive ICs and external connections. Therefore, lower price and compacter TFT LCDs should be realized in the near future.

Use of conventional glass substrates is also advantageous for reducing TFT fabrication costs, though high temperature glass substrate has been tentatively used to fabricate high temperature poly-Si TFTs [5]. To realize TFTs on hard glass substrate, the maximum process temperature must be below 600 ℃.

Under this limitation, a high quality active layer poly-Si is an indispensable component to realize high-performance poly-Si TFTs. Generally, low pressure chemical vapor deposition (LPCVD) poly-Si and simple thermal annealing for recrystallization have been used [3,6,7]. To obtain higher quality poly-Si, reduction of atomic defects (dangling bonds) and improvement of crystallinity are necessary.

In this paper, effective hydrogenation by H_2 plasma using a thin poly-Si gate and optimization of poly-Si deposition conditions were studied. Furthermore, the developed TFTs were applied to TFT LCDs to confirm the capability of monolithic drive circuits integration.

TFT FABRICATION

Figure 1 shows a cross-sectional view of the poly-Si TFT with the conventional n-channel MOS FET structure. An under layer of SiO_2 was deposited by atmospheric pressure chemical vapor deposition (APCVD) on a hard glass substrate (100×100 mm^2). Poly-Si (1500 Å thick) was deposited at 620-630 ℃ by LPCVD to give the active layer poly-Si. The poly-Si was annealed to be recrystallized at 600 ℃ for 20 h in N_2. The poly-Si was patterned into islands. Gate oxide (1000 Å) was deposited by APCVD . Gate poly-Si (500-3500 Å) was deposited by LPCVD at 550 ℃. After gate patterning, phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} and 30 keV to form the source and drain region. After deposition of phospho-silicate glass (PSG) for passivation, thermal annealing was carried out at 600 ℃ for 20 h in N_2 to activate implanted ions. After metallization by sputtered AlSi(2%), the substrate was annealed at 400 ℃ for 30 min in the forming gas. Finally, hydrogenation was carried out in a plasma reactor (13.56 MH_z) at 300 ℃.

IMPROVEMENT OF HYDROGENATION EFFECT

Figure 2 shows hydrogenation effect on threshold voltage vs. gate poly-Si thickness characteristics. Thinning of gate poly-Si was remarkably effective in reducing the threshold voltage. The reduction ratio is about 50% at the gate poly-Si thickness of 1000 Å.

Figure 3 shows the hydrogenation effect on field effect mobility vs. gate poly-Si thickness characteristics. The field effect mobility also increased in the thin poly-Si gate TFTs.

Futher thinning of the gate (below 500 Å) may be more effective, however, the sheet resistance of

436-IEDM 87

gate poly-Si increased. Therefore the Gate poly-Si thickness of 1000 Å was adopted in this study.

OPTIMIZATION OF POLY-Si DEPOSITION CONDITIONS

Figure 4 plots dependence of X-ray diffraction intensity of (111) surface on poly-Si deposition temperature. The intensity was used as an indicator for crystallinity of the poly-Si layer. The poly-Si deposited below 560 ℃ was amorphous. After thermal annealing at 600 ℃, the poly-Si deposited at 550-560 ℃ showed the highest intensity indicating that it had the highest crystallinity (mean grain size : 200 Å). This was assumed that nucleation in the deposition process and recrystallization in annealing were optimal for the Si film deposited at 550-560 ℃.

Figure 5 plots dependence of field effect mobility and threshold voltage on poly-Si deposition temperature. In this experiment, the gate thickness was 3500 Å, therefore hydrogenation was not applied. The field effect mobility became a maximum (30 $cm^2/V \cdot s$) and threshold voltage became a minimum (12 V) at the deposition temperature of about 550 ℃. These results agree with the results of Figure 4.

TFT CHARACTERISTICS

Figure 6 shows the drain current-gate voltage characteristics of the TFT which had an optimum structure with poly-Si deposited at 550 ℃ and thin gate of 1000 Å. The on-current was remarkably improved by hydrogenation when high quality poly-Si was used. It was noteworthy that the curve had a flat bottom in the gate voltage region of -10 to 0 V. The off-current was constant and independent of the channel length (5-120 μm). This indicated that off-current in the flat region depended only on the characteristics of n^+-i junction and that the main component of the leakage current was the generation current in depletion layer. Therefore, the leakage current should be reduced by reducing the trap density and thinning the active layer poly-Si.

Figure 7 shows drain current-gate voltage characteristics of TFT with poly-Si deposited at 520 ℃. The on and off-current characteristics were also improved. But in this figure, the TFT with low quality poly-Si did not have flat bottom behavior.

Table 1 summarizes the characteristics of the TFTs with optimized-temperature (550 ℃)-deposited poly-Si and thin gate (1000 Å).

APPLICATION FOR LOGIC CIRCUITS AND LCD

Table 2 summarizes the characteristics of 51-stage ring oscillators. This high speed operation showed the possibility for composing logic circuits with the developed TFTs [4].

Figure 8 shows schematic diagram of the drive circuits integrated display which had a display area with a 3.3" diagonal and 386(H)×133(V) dots.

Figure 9 shows multi-color diplay image of poly-Si TFT LCD with fully integrated drive circuits. Whole diplay area was drived by monolithically-integrated drive circuits with supply voltage of 20 V.

SUMMARY

High-performance low-temperature poly-Si TFTs were developed by a 600 ℃ process on glass substrate. Threshold voltage was remarkably reduced using a thin gate (1000 Å) by H_2 plasma hydrogenation. X-ray diffraction intensity (an indicator of crystallinity) of poly-Si depended closely on poly-Si deposition temperature and showed maximum at 550-560 ℃. The developed TFTs with poly-Si deposited at 550 ℃ and a thin gate of 1000 Å had the V_{TH} of 6.2 V and μ_{FE} of 37 $cm^2/V \cdot s$. These TFTs should be used to realize LCDs with monolithically-integrated data and scan drive circuits.

ACKNOWLEDGEMENTS

The authors wish to thank Dr. Y. Kawamoto, Dr. E. Kaneko, Mr. H. Hisada, Mr. R. Nashimoto, Mr. H. Suzuki, and Dr. K. Suzuki for their guidance and encouragement. They also like to thank Mr. H. Nagano, Dr. Y. Okajima, Mr. T. Aoyama, Mr S. Oikawa and Mr. M. Takabatake for their help in the device fabrication.

REFERENCES

[1] J. Ohwada, H. Kawakami, Y. Nagao, Y. A. Ono, K. Ono, A. Misura, and N. Konishi : SID 87 DIGEST, p. 55 (1987).

[2] Y. Oana : SID 84 DIGEST, p. 312 (1984).

[3] S. Morozumi, K. Oguchi, T. Misawa, R. Araki, and H. Ohshima : SID 84 DIGEST p. 316 (1984).

[4] J. Ohwada, M. Takabatake, H. Kawakami, Y. A. Ono, A. Misura, K. Ono, N. Konishi, T. Suzuki, and K. Miyata : Extended Abstract of the 1987(19th) Conference on Solid State Devices and Materials, p. 55 (1987).

[5] J. R. Troxell, M. I. Harrington, J. C. Erskin, W. H. Dumbaugh, F. P. Fehlner, and R. A. Miller : IEEE ELECTRON DEVICE LETTERS, EDL-7, p. 597 (1986).

[6] S. Morozumi, R. Araki, H. Ohshima, M. Matsuo, T. Nakazawa, and M. Sato : JAPAN DISPLAY '86 p. 196 (1986).

[7] M. Bryer, P. Cozon, G. Fortunato, R. Kean, D. Meakin, P. Migliorato, P. Rundle, and H. Urwin : JAPAN DISPLAY '86, p. 80 (1986).

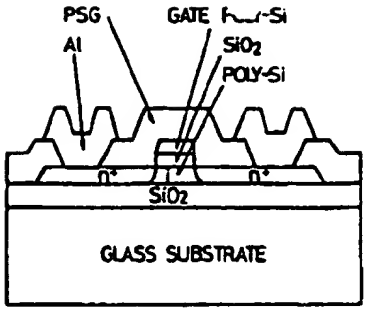


Fig. 1 Cross Section of Poly-Si TFT.

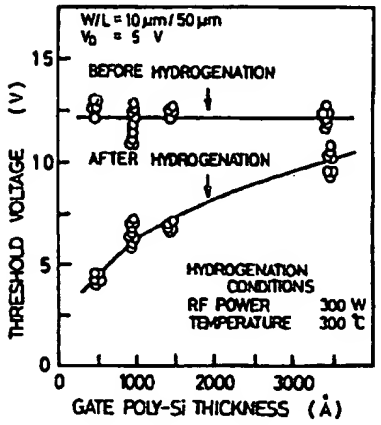


Fig. 2 Hydrogenation Effect on Threshold Voltage vs. Gate Poly-Si Thickness Characteristics.

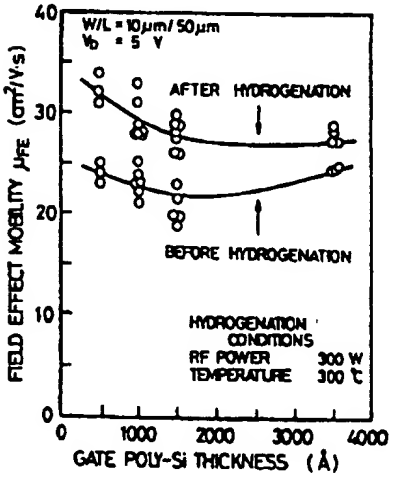


Fig.3 Hydrogenation Effect on Field Effect Mobility vs. Gate Poly-Si Thickness Characteristics.

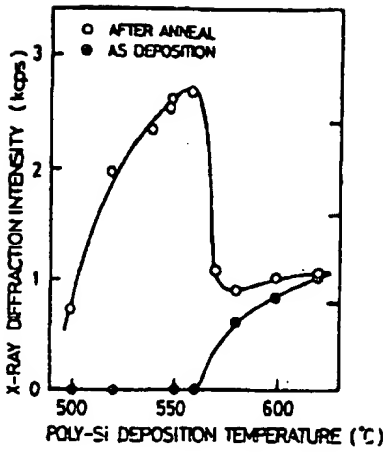


Fig. 4 Dependence of X-ray Diffraction Intensity of (111) Surface on Poly-Si Deposition Temperature.

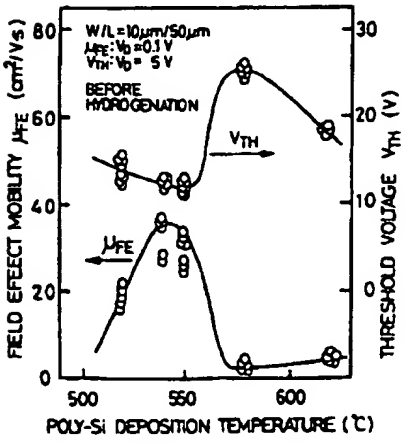


Fig. 5 Dependence of Field Effect Mobility and Threshold Voltage on Poly-Si Deposition Temperature.

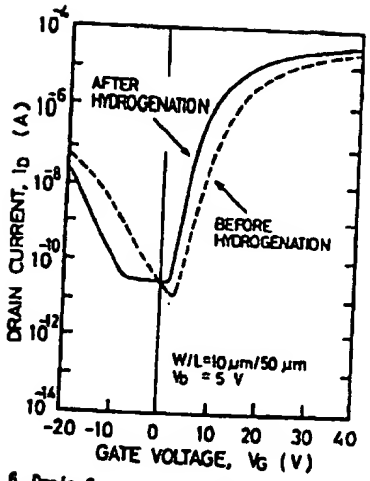


Fig. 6 Drain Current-Gate Voltage Characteristics of Poly-Si TFT.
Poly-Si Deposition Temperature : 550℃
Gate Poly-Si Thickness : 1000 Å

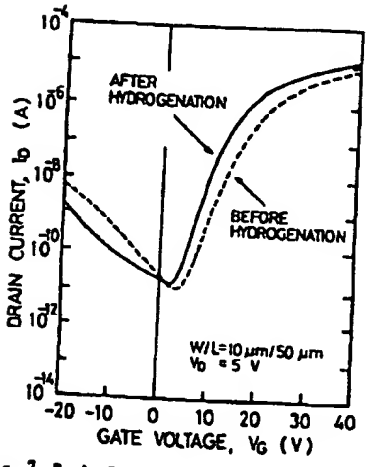


Fig. 7 Drain Current-Gate Voltage Characteristics of Poly-Si TFT.
Poly-Si Deposition Temperature : 520 ℃
Gate Poly-Si Thickness : 1000 Å

Table 1 Characteristics of the Developed TFT with Optimized Temperature Deposited Poly-Si and Thin Gate.

THRESHOLD VOLTAGE	6.2	V	(V_D=5 V)
FIELD EFFECT MOBILITY	37	$cm^2/V \cdot s$	(V_D=0.1 V)
ON-OFF CURRENT RATIO	6.3×10^5		(V_D=5 V, V_G=20.0 V)
OFF CURRENT	2.7×10^{-11}	A	(V_D=5 V, V_G=0 V)

Table 2 Characteristics of 51-Stage Ring Oscillators.

TYPE	A	B
LOAD TFT W/L	30μm/60μm	30μm/30μm
DRIVE TFT W/L	50μm/10μm	50μm/ 5 μm
DELAY TIME / STAGE (V_{DD}= 30 V)	75 ns	11 ns
POWER / STAGE (V_{DD}=30 V)	2.1 mW	4.7 mW

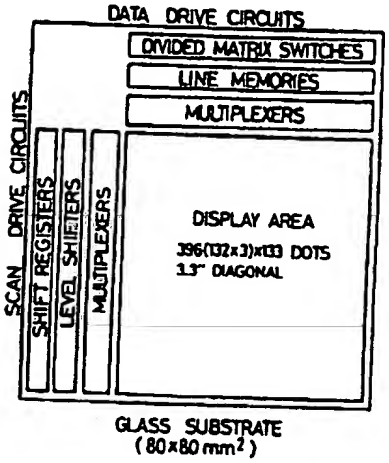


Fig. 8 Schematic Diagram of Drive Cicuits Integrated Display.

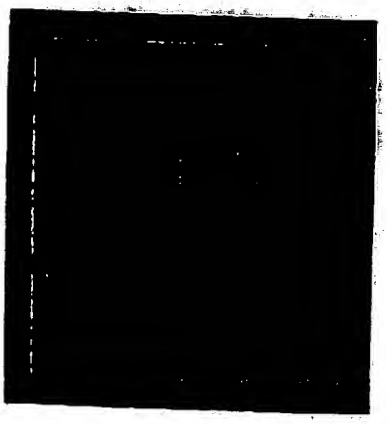


Fig. 9 Multi-Color Display Image of Poly-Si TFT LCD with Fully Integrated Drive Circuits.

IEDM 87-439